

Patent claims

1. A method of controlling a data transmission memory (1) for the transmission of data packets between subscribers T in which a chained subscriber-pointer address list with address pointers for addressing data memory blocks of a data memory (3) is stored for each subscriber T in a pointer address memory (2).
2. The method as claimed in claim 1, in which each data memory block comprises a plurality of data memory cells.
- Sub 3. The method as claimed in claim 1 or 2, wherein the number of data memory cells contained in the data memory block corresponds to the number of subscribers.
4. The method as claimed in one of the preceding claims, in which, in a reception operating mode, reception data packets are received from various source subscribers via a reception data bus and are stored in data memory cells of a data memory block addressed by the subscriber-pointer address list.
5. The method as claimed in one of the preceding claims, in which, in a transmission operating mode, output data packets are in each case read out from a data memory block and sent to the associated destination subscriber via an output data bus.
6. The method as claimed in one of the preceding claims, in which each reception data packet contains destination information data for identifying that destination subscriber for which the reception data packet is intended.
7. The method as claimed in one of the preceding claims, in which the memory size of a data memory cell corresponds to the size of an input data packet and the memory size of a data memory block preferably corresponds to the size of an output data packet.
8. The method as claimed in one of the preceding claims, in which the state of each chained subscriber-pointer address list is stored in a subscriber state register (12).

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data block.

16. The method as claimed in one of the preceding claims, in which the reception operating mode for writing reception data packets into the data transmission memory (1) has priority over the transmission operating mode for sending output data packets from the data transmission memory (1).

17. A data transmission memory (1) for the transmission of data packets between subscribers T with a pointer address memory (2) for storing chained subscriber-pointer address lists, comprising pointer addresses, for each subscriber; a plurality of subscriber state registers (12), which in each case store the state of an associated subscriber-pointer address list; a data memory (3) for storing data blocks which can be addressed by the pointer addresses; and with a memory controller (4) for controlling the pointer address memory (2) and the data memory (3).

18. The data transmission memory as claimed in claim 17, wherein the data memory (3) is a SRAM.

19. The data transmission memory as claimed in claim 17, wherein the pointer address memory (2) is a SRAM.

20. The data transmission memory as claimed in one of the preceding claims, wherein the memory controller (4) is connected to source subscribers via a reception data bus and to destination subscribers via a transmission data bus.

21. The data transmission memory as claimed in one of the preceding claims, wherein the transmission data bus and reception data bus are bidirectional buses for bidirectional data transmission.

22. The data transmission memory as claimed in one of the preceding claims, wherein the buses are Ethernet buses.

A1 Cont.

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A2